REMARKS

Applicant thanks the Examiner for the courtesies extended to the undersigned during the telephone interview on October 2, 2003.

The application has been reviewed in light of the Office Action dated July 15, 2003. Claims 1-9 are pending, with claim 9 having been withdrawn by the Patent Office from consideration. By this Amendment, Applicant has amended independent claim 1 to clarify the claimed invention and place the claims in better form for examination. Applicant respectfully submits that no new matter is introduced by the claim amendments. Accordingly, claims 1-8 are presented for consideration, with claim 1 being in independent form.

The drawings are proposed to be amended by adding new FIG. 7 which is attached hereto as Exhibit A. Support for FIG. 7 can be found in the specification at, *inter alia*, page 13, lines 11-22.

The specification is proposed to be amended to incorporate reference to the proposed FIG. 7.

Claims 1-3, 5, 7 and 8 were rejected under 35 U.S.C. §102(b) as purportedly anticipated by U.S. Patent No. 4,804,636 to Groover III et al. Claims 1-3 and 5-8 were rejected under 35 U.S.C. §102(e) as allegedly anticipated by U.S. Patent No. 5,911,114 to Naem. Claim 4 was rejected under 35 U.S.C. §103(a) as purportedly unpatentable over U.S. Patent No. 5,911,114 to Naem.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claim 1, as amended, is patentable over the cited art, for at least the following reasons.

The present application relates to resistance patterns for a semiconductor device wherein resistance variance (of the resistance

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element) caused by imprecision of patterning the resistance pattern is minimized.

For example, claim 1 recites a semiconductor device which comprises a Si substrate and a resistance element formed on the Si substrate. The resistance element includes a plurality of first resistance patterns of silicide and a second resistance pattern of silicide. The first resistance patterns of silicide are provided on the substrate at a first level and are arranged in parallel with each other with a mutual separation. The second resistance pattern of silicide is provided adjacent to and between the first resistance patterns at a second level lower than the first level, is electrically connected in series to the first resistance patterns to form the resistance element, and has an edge defined by the first resistance patterns. Each of the first resistance patterns and second resistance pattern has a substantially identical length, and each second resistance pattern is disposed between a corresponding pair of first resistance patterns, such that the first and second resistance patterns are configured in a complementary arrangement in an alternating sequence. As discussed in the application at, for example, pages 7 and 13, the complementary arrangement of the first and second resistance patterns in such manner effectively compensates for any resistance change caused by size variation of the first resistance pattern.

Applicant finds no teaching or suggestion of the claimed invention in the art.

Groover, as understood by Applicant, relates to interconnect technology for VLSI integrated circuits. According to Groover, first poly, second poly and moat are all interconnected in a desired pattern by TiN local interconnect.

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The Office Action states that Groover discloses a plurality of poly-Si first resistance patterns and a $TiSi_2$ second resistance pattern. Fig. 8 of Groover were cited in the Office Action as showing first resistance patterns arranged in parallel with each other with mutual separation.

Applicant does not find teaching or suggestion in Groover, however, that each of the first resistance patterns and second resistance pattern has a substantially identical length, and each second resistance pattern is disposed between a corresponding pair of first resistance patterns, such that the first and second resistance patterns are configured in a complementary arrangement in an alternating sequence.

Naem, as understood by Applicant, relates to a method of simultaneously forming refractory metal salicide and a local interconnect.

The Office Action states that Naem discloses a semiconductor device comprising a plurality of salicide first resistance patterns on the field oxide region of the device and a salicide second resistance pattern on the source and drain. The Office Action further states that Naem discloses that the second resistance pattern is formed in the substrate in the form of a salicide region defined by the first resistance pattern.

However, Applicant finds no teaching or suggestion in the cited art of a semiconductor device which comprises a Si substrate and a resistance element formed on the Si substrate, wherein the resistance element includes a plurality of first resistance patterns of silicide and a second resistance pattern of silicide, the first resistance patterns of silicide are provided on the substrate at a first level and

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are arranged in parallel with each other with a mutual separation, the second resistance pattern of silicide is provided adjacent to and between the first resistance patterns at a second level lower than the first level, is electrically connected in series to the first resistance patterns to form the resistance element, and has an edge defined by the first resistance patterns, each of the first resistance patterns and second resistance pattern has a substantially identical length, and each second resistance pattern is disposed between a corresponding pair of first resistance patterns, such that the first and second resistance patterns are configured in a complementary arrangement in an alternating sequence, as provided by the invention recited in amended claim 1. The cited art simply does not disclose or suggest that the complementary arrangement of the first and second resistance patterns in such manner can effectively compensate for any resistance change caused by size variation of the first resistance pattern.

Accordingly, for at least the above-stated reasons, Applicant respectfully submits that independent claim 1, and the claims depending therefrom, are patentable over the cited references.

The Office is hereby authorized to charge any fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition, and the Commissioner is authorized to charge the requisite fees to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the

undersigned attorney.

Entry of this amendment and allowance of this application are respectfully requested.

Respectfully submitted,

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